Technology Offer

Single Photon Detection: Advanced DePFET with High Amplification

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The invention relates to a new and improved concept for Depleted p-channel Field Effect Transistors (DePFET) detectors that provides a significantly higher intrinsic amplification. By the extension of the transistor layout, former limitations were overcome.

DePFETs are insufficient for many applications in terms of the achievable intrinsic amplification. This is since shorter transistor channels needed for high amplification would increase the detector noise caused by impact ionization events.

Additional resistive components were introduced in order to lower the voltage drop in the DePFET's internal gate which enabled shorter channels at sufficient noise levels. The new concept allows for the construction of photodetectors sensitive to single photons.

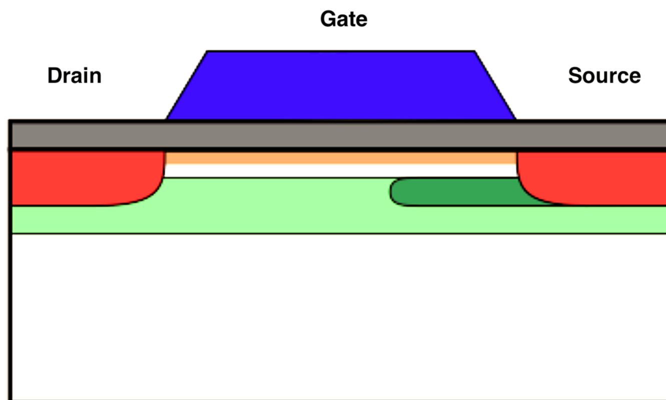

Fig. 1: The cross-section of an improved DePFET according to the invention is similar to state-of-the-art products. The additional n-implant is colored in dark green (see below).

Advantages

- Simple to manufacture extension to the well proven DePFET concept
- Quicker and less losses than in CCD detectors
- Single photon detection possible
- Increased amplification by a factor of 5 compared to other DePFET detectors
- Transistor current of more than 2 nA per signal electron

Applications

- Single Photon detection
- X-Ray imaging
- Industrial quality inspections
- High energy physics, Particle detectors
- Astronomy

Background

DePFETs are well known components used in detector assemblies since decades as they possess high intrinsic charge amplification combined with low noise levels resulting in excellent SNR values. The charge multiplication however is limited by the geometry of the internal gate. A further improved gain would be favorable for various detector applications, but an even smaller gate size would lead to higher electric fields and thus increased noise, making this approach inappropriate.

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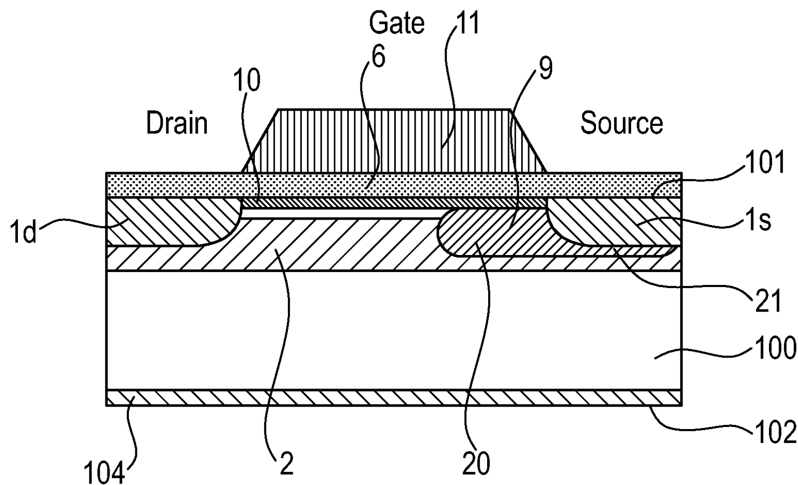

Fig. 1: A schematic drawing of an improved DePFET device shows the arrangement with an additional n implant (20) that localizes the internal gate and reduces the voltage drop inside the transistor.

Technology

An advancement of the current DePFET principle has been developed to overcome the aforementioned shortcomings and to further expand the application possibilities of DePFET detectors. As the fundamental constraint is purely a result from the high potential drop over small distances for improved internal gate geometries, the invention is based on the use of additional implants over which a portion of the Drain-Source-Voltage can drop. This allows to reduce the internal gate length significantly and hence improve the amplification.
A possible implementation of the invention can be seen in figure 2. Within the main substrate (100), limited by its two surfaces (101, 102), it comprises the drain and the source terminal (1d, 1s), as well as a doping increased region (2) and the channel region (10). The latter is located beneath the gate electrode (11) and the gate insulator (6). The rear activation region (104) is located on the opposite side.
According to the invention, the key component used to reduce the internal gate size is the additional n-implant (20) which localizes the internal gate and decouples its size from the one of the external gate without increasing the detector noise.

Patent Information

PCT *(WO2020225275A1)*, EPO *(EP3942619A1)*, DPMA *(DE102019206494A1)*

Publications

A. Bähr*, et al.*, " Advanced DePFET concepts: super gq DePFET", Proc. of SPIE Vol. 11454 (2020).

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